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Toward sub-micron pixels for short-wave infrared imaging

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Abstract
The sensitivity of infrared (IR) imagers can be significantly improved by reducing the size of photodetectors down to the diffraction limit. Emerging low-dimensional material enable submicron photodetectors, which can be diffraction limited and lead to significant sensitivity improvement in the critical short-wave IR band. However, reaching this limit requires pixel sizes smaller than the metal bumps needed for hybridization to silicon readout chips. Such tiny fragile pixels are susceptible to damages due to the mechanical pressure applied during flip-chip bonding, degrading the number of functional camera pixels. Herein, we systematically characterize the influence of the detector size on the imager pixel yield. We then introduce strategies for improving the yield of sub-micron pixels from less than half of total pixels to more than 3/4 of them. While we used a top-down fabrication for our detectors, the developed method is also applicable to bottom-up fabrication methods to make highly sensitive IR cameras based on emerging low-dimensional material such as catalyst-assisted nanowires.

Keywords: SWIR FPA, diffraction limited pixel size, hybridization, flip-chip bonding, operability, indium bumping

(Some figures may appear in colour only in the online journal)

1. Introduction

Imaging sensors technology has been evolving toward smaller pixels for improving resolution and for reducing the cost and the size, weight, and power consumption of the system and optics [1–3]. In addition, scaling down the pixel photodetector while compensating the optical fill factor by using light coupling system results in an increased level of specific detectivity thanks to the reduction of junction capacitance and dark current [4–7]. The specific detectivity is defined as:

$$D^* = \frac{\lambda}{hc}\eta\sqrt{\frac{1}{2(G+R)t}\cdot\frac{A_o}{A_e}} \quad (1)$$

where, hc/λ and η are the energy of the absorbed photons and the detectors quantum efficiency, respectively. G, R, and t are the excess carrier generation, recombination rates, and the thickness of the detector, respectively. A_e and A_o are the electrical and optical active areas.

However, the challenges of coupling light to excessively small detectors cause a decrease in quantum efficiency and impose more stringent requirements on the optics of the system. This trade-off results in an optimal pixel size for imaging sensors, which was theoretically demonstrated to coincide with the diffraction limit size [1, 2]. Hence, to date, reaching diffraction-limited pixel size has been a common goal for all imaging sensors. Current visible-image sensors employed in commercial mobile cameras have pixel sizes ranging between 1 and 2 μm, and complementary metal oxide semiconductor (CMOS) image sensors have recently been developed with

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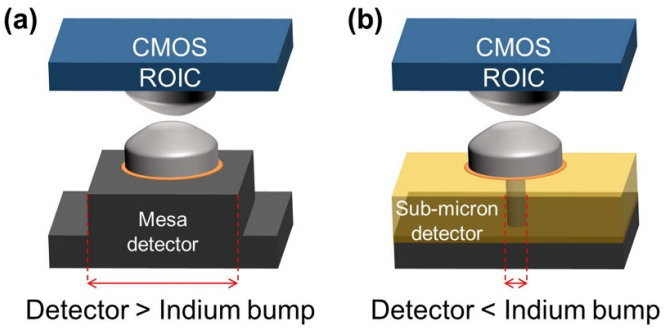

Figure 1. Conceptual schematics showing the hybridization process of (a) a typical mesa-type pixel structure, and (b) a sub-micron pixel structure smaller than an indium bump.

0.7 μm pixels, both of which approach the diffraction limit at their respective detection wavelengths [8, 9]. Meanwhile, the detector size of infrared (IR) image sensors is currently limited to 4–5 μm regardless of the detection wavelength band [10, 11]. This is mainly because the fabrication of IR imagers typically requires hybridization of the focal plane array (FPA) with the CMOS read-out integrated circuit (ROIC), which are different material systems and substrates. This hybridization is accomplished by thick metal bumps, which stably connect each pixel of the detector array with the corresponding read-out pad of the ROIC (see figure 1(a)) [12]. As a result, the pixel size of most IR FPAs has been limited by the minimum achievable bump size rather than by the limits of very-large-scale integration fabrication technology [13, 14]. This limitation does not prevent diffraction-limited pixel sizes in either mid-wave IR (3–5 μm) or long-wave IR (8–12 μm) imagers. In the case of short-wave (SW) IR (1–3 μm) imagers, however, this pixel size limitation has hampered the potential performance improvements enabled by further reducing the pixel size [4].

A potential solution to achieve the diffraction-limited size in SWIR FPAs consists of scaling down the pixel size while maintaining the pixel-pitch, as shown in figure 1(b). Few such attempts have been made, however, due to two main challenges. First, this reduction in size of the detectors results in shrinking the pixel's photosensitive area, hindering the efficiency of light collection over the pixel area (fill factor), and thus reducing the quantum efficiency [4]. The second challenge is in the fabrication: as the pixel size becomes smaller than the indium bump, a complicated planarization process is required to safely stack large indium bumps on top of the small pixels. In addition, even once the bumps are formed on the detector, the mechanical pressure applied during the flip-chip process can cause mechanical damage or rupture of the sub-micron detector structures. This condition leads to reduction of the FPA operability. Here, the operability is defined as the percentage of fully functional pixels with respect to all pixels in the FPA. While the fill factor issue can be addressed by using light concentrators as reported in several studies [15–19], the structural issue has not been addressed yet. Therefore, this study will focus mainly on the second challenge. We characterize the effect of scaling down the pixel size of SWIR FPAs on their operability, and investigate the origin of the issue. We then utilize several fabrication and hybridization strategies to enhance the structural stability of sub-micron pixel during flip chip bonding, and demonstrate relatively high operability for sub-micron detectors for the first time. We believe that the proposed strategies will provide significant insights in realizing next generation imaging sensors [20] and microdisplays [21] that employ various optoelectronic devices composed of nanostructures.

2. Experiments

2.1. Device fabrication

In this study, results from two different SWIR FPAs are presented. One FPA was designed to investigate the influence of pixel size on operability, while the second was designed to evaluate a strategy we have developed to improve the structural stability of sub-micron pixels, as explained in the following section.

Figures 2(a)–(d) show schematics of the fabrication process of a SWIR FPA based on sub-micron pixel photodetectors. For both FPAs, we use an *n–p–n* InGaAs/InP heterojunction phototransistor (HPT) structure that we have developed in our previous study [22]. First, to achieve low resistance ohmic contacts, a metal stack (Ti/Mo/Au/Cr), which serves both as top ohmic contact and etching mask [23], was formed on the InGaAs cap layer using electron beam lithography and electron beam evaporation. Then, *n–p–n* HPT pillars were defined via CH_4/H_2-based reactive-ion etching (RIE). Figure 3(a) shows scanning electron microscope (SEM) images of HPT pillars with diameters of 1 μm and 500 nm right after the RIE. As shown in the SEM images, it can be seen that a sidewall of the metal stack is very rough, which indicates that a polymer is formed on the sidewall of the metal during the RIE [24]. Such a polymer unintendedly acts as an additional etch mask during the dry etching process and thus roughen the sidewall of HPTs, thereby degrading their electrical performance. In order to remove the polymer and repair the surface damaged from RIE, a phosphoric acid-based wet chemical treatment was processed. Comparing the SEM images of figures 3(a) and (b), the polymer was completely removed and the sidewall of HPTs became smooth after the wet chemical treatment.

However, the wet chemical treatment inevitably causes undercuts on the sidewall of HPTs due to isotropic etching. The undercut phenomenon does not matter in terms of fabrication compatibility when realizing typical FPAs consisting of a relatively large detector of several tens of micrometers or more, but it makes the reliable flip-chip bonding process challenging in case of submicron-sized detectors due to their high aspect ratio. We investigated the diameter of HPTs reduced by undercut to find the size of HPTs compatible with flip-chip bonding. Under our optimized wet treatment condition, the diameter of the active region (base layer) of HPTs was reduced by 350 nm after the treatment (figure 3). Therefore, the active

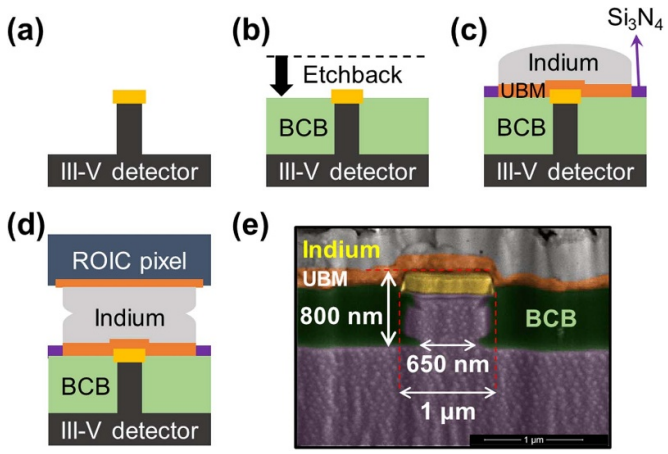

Figure 2. Schematics of the fabrication process of SWIR FPAs consisting of sub-micron pixels: (a) dry and wet etching, (b) planarization by BCB coating and etch-back process, (c) indium bump formation by electroplating, (d) flip-chip bonding process for interconnecting the ROIC and detector array. (e) A cross-sectional SEM image of a 1 μm pixel after the formation of the indium bump. The active region of the pillar has a 650 nm-diameter.

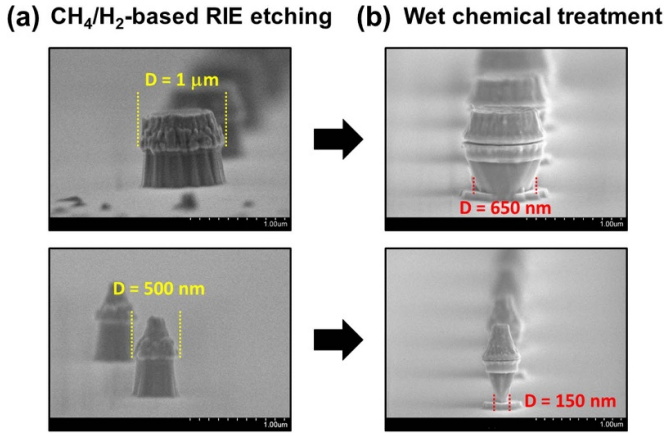

Figure 3. Tilt-view SEM images showing (a) HPT pillars after CH_4/H_2-based RIE etching, and (b) HPT pillars after wet-chemical treatment.

region diameters of HPTs with the mask diameters of 1 μm and 500 nm were reduced to 650 nm and 150 nm, respectively.

Before the full-scale experiment, we made a test sample to find the minimum mask diameter below which the HPT operation is heavily affected by its surface. We observed that HPT pillars with the mask diameters of 500 nm were heavily affected by their surface, but HPT pillars with the diameters of 1 μm operated normally. Based on this test, HPT pillars with the mask diameter of 1 μm were set as the representative size in this study. Note that the diameter of the active region (base layer) of pillars is significantly smaller than the mask due to the undercut etching by the wet-chemical etchant. For the devices with 1 μm mask, the actual InGaAs base diameter is about 650 nm (see figure 2(e)). Considering the actual diameters, these devices in our study are good representatives of sub-micron devices.

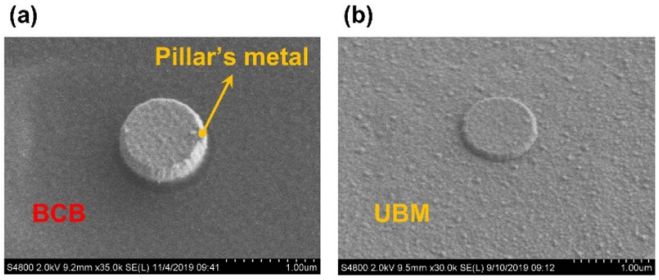

Figure 4. Tilt-view SEM images showing (a) the metal stack of a HPT pillar exposed after BCB etch-back process, and (b) an under bump metallization (UBM) layer that covered the HPT pillar's metal stack and the surrounding BCB planarization layer.

After the wet etching, benzocyclobutene (BCB) was then spin-coated on the detector sample, acting both as passivation and planarization layer. Accurate RIE (SF_6/O_2) etch-back allows us to expose only the metal layer from the HPT pillars (figure 2(b)). We developed a method to accurately etch-back the BCB layer across every pixel. The SEM image in figure 4(a) shows that the metal stack (Ti/Mo/Au/Cr) was fully exposed without over-etching for a single detector with a diameter of 1 μm after the etch-back process. Considering that the thickness of the metal stack is about 230 nm, it can be estimated how accurate our etch-back process is. Following the etch-back process, under bump metallization (UBM) layers were deposited on submicron-sized HPTs and the surrounding BCB layer (figure 4(b)). The UBM layers serve as a reliable bridge between the submicron-sized detectors and the indium bumps with a diameter of 10 μm, allowing for an electrically stable connection.

Next, we deposited a 100 nm thick Si_3N_4 passivation layer on BCB layer to prevent gas-releasing of BCB material. After forming the indium bumps on the respective pixels (320 $\times$ 256/30 μm pitch) of the FPAs and ROICs chips by standard electroplating bump process, they were aligned and bonded using a SET FC150 flip-chip bonder, at 20 kg pressure and 110 °C (figure 2(d)).

2.2. Device measurement

The operability of the fabricated FPAs was obtained by identifying damaged and normal pixels. A pixel was considered functional only if it was both well-connected to the ROIC and had a flat-field gain above 1. To assess connectivity, the pixel response to zero illumination was measured as a function of integration time. A response linearly proportional to the integration time confirms the pixel is able to send dark current to the ROIC, whereas jagged or non-increasing behavior indicates a disconnect. To assess gain, pixels were illuminated with pulses of calibrated diffuse 1550 nm light and the peak-to-peak response swing was measured. The gain must be above one electron per photon incident on the pixel area to be acceptable. Both conditions are necessary: a short-circuited pixel can register as connected despite lacking photo-response, and intermittent pixels can have photo-response without reliable connectivity.

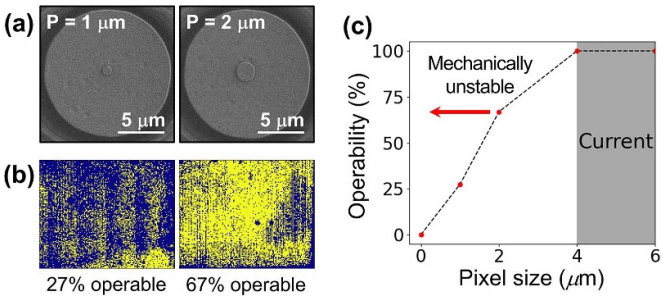

Figure 5. (a) SEM images of 1 μm (left) and 2 μm (right) diameter pillars. (b) Maps of the respective FPA regions. Yellow is functioning, blue is damaged. (b) Operability depending on pixel size. Larger pillars are more stable.

3. Results and discussion

3.1. Pixel operability depending on photodetector size

The first FPA was designed to include two different regions consisting of pixel sizes of 1 and 2 μm (figures 5(a) and (b)), so as to investigate the pixel operability depending on their size. Figure 5(b) shows a map of pixel operability in each region, where yellow pixels are functional and blue are damaged. In the region consisting of 2 μm pixel detectors, about two thirds of the pixels are fully functional (66.9%), while for the 1 μm pixels the operability is below one third (27.4%). Figure 5(c) shows the plot indicating pixel operability as a function of size: the operability drops sharply below 2 μm. In short, operability decreases as the pixel size becomes smaller. To find the exact cause of the decrease in pixel operability, we investigated the main processes that can reduce operability. In this experiment, since the two different regions were fabricated on the same FPA chip, there was no difference in fabrication between the two regions. As a result, only two processes could have affected the operability in relation to the size differences in the pixel detectors: (a) planarization or (b) flip-chip bonding. In the planarization process, polymer coatings on regions with different pattern designs can result in non-uniform coating films, reducing operability. However, we confirmed the accuracy of the planarization process across the entire area of the sample, regardless of the pixel size, as shown in SEM images in figures 2(e) and 4(b). Conversely, it is reasonable to expect that small pixels can be damaged or broken by the mechanical pressure applied during the flip-chip process due to their high aspect ratio. This is further validated by the trend of larger pixels with more structural stability having higher operability. We concluded that the operability reduction is mainly due to the flip-chip bonding process rather than the planarization process.

3.2. Strategies for improving the operability of scaled photodetectors

In light of this result, the second FPA was designed to show the relationship between pixel operability and the mechanical

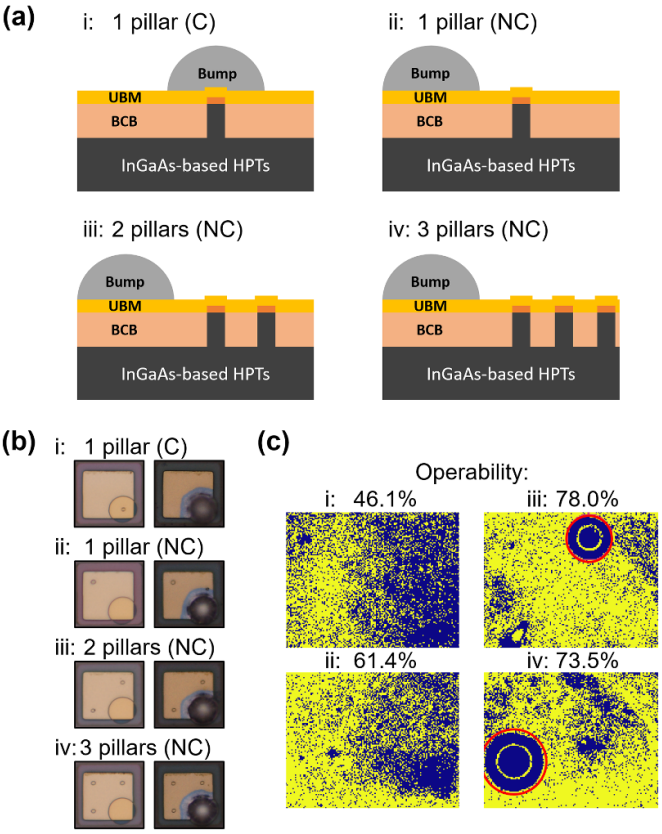

Figure 6. (a) Connectional schematics of four different 1 μm pixel designs: (i) a single detector structure covered by the indium bump; and (ii) single, (iii) double, and (iv) triple detector structure not covered by the indium bump. (b) Microscope images of the representative pixels and (c) the pixel operability in regions containing each design. Yellow pixels are functioning, and blue pixels are damaged. The red outline shows zones excluded from consideration due to obvious processing defects unrelated to pixel design.

pressure applied on the pixel during bonding. At the same time, this imager also tested two strategies for improving the structural stability of small pixels. The FPA is composed of four regions with different geometric configurations (i–iv) as shown in figure 6(a). Each region tested a different position of the indium bumps relative to the pixels' injector pillars or a different number of pillars per bump, in order to compare the differences in structural stability. All processing conditions, including the mechanical pressure for flip-chip bonding, were kept the same as for the first FPA.

The first strategy for improving pixel stability was to offset the location of the small detector within the pixel area with respect to the indium bump, as shown in figure 6(ai) versus figure 6(aii). Here, 'C' refers to the structure in which indium bumps cover the detectors, while 'NC' refers to the structure in which indium bumps did not cover the detectors. The 'NC' design allows the bumps and pixels to be electrically connected while alleviating the mechanical pressure being applied directly to the small pillars. When comparing the response of the pixels over these two regions, shown in figures 6(ci) and

(cii), it is evident that this strategy successfully alleviates the mechanical pressure, thereby improving the pixel operability from 46.1% to 61.4%. However, even when the indium bump is not placed directly on top of the pixels, the operability is still not optimal. We believe that some of the applied pressure may be transmitted to the detector structures via shear motion in the BCB polymer layer.

To further enhance the structural stability, the second strategy we investigated involved placing multiple detector structures connected in parallel to form one pixel. This approach reduces the shear force per device, providing a more stable structure than a single structure of the same cross-sectional area. Figures 6(aii)–(aiv) show the single, double, and triple structures, respectively, all having an offset from the indium bump. Multi-detector structures significantly improved the operability compared to the single-detector structure. In the regions with double (78.0%) and triple structures (73.5%), three quarters of all pixels operate correctly. This is quite a large value when considering the very small size of the devices and that the fabrication was performed manually, especially compared to the 1 μm pixels on the first FPA.

In this study, the multi-detector structure was employed in terms of improving operability, but it can also be beneficial in terms of sensitivity. Our previous research experimentally proved that the fill factor of such multi-detectors can be considerably improved by appropriate spacing of the detectors within the diffusion length of the photogenerated excess carriers [25]. However, too many detectors introduce problems of their own. As the number of structures increases, the pixel's total dark current also increases; and our second FPA shows that triple detectors showed a slightly lower operability than double detectors (73.5% vs. 78.0%). Therefore, the appropriate number of structures and their spacing requires optimization to obtain both high operability and sensitivity [26]. In addition, the mechanical pressure and temperature condition of the flip-chip bonding process can also be optimized for sub-micron pixels, in order to achieve high pixel operability with a minimum number of detector structures.

4. Conclusion

We have evaluated the main reasons for low operability of sub-micron detectors when hybridized with silicon readout using indium bump-bonding. We developed strategies to address the sources of damage, and demonstrated a SWIR FPA consisting of sub-micron photodetectors with high operability. Our experimental results show that as the size of the pixel decreased below 2 μm, the operability of FPA was severely reduced. In order to address this issue, the indium bump location was designed to have an offset from the sub-micron detector structure within each pixel. In addition, we fabricated parallel multiple-detectors to reduce the stress of each detector. By employing both strategies, a significant operability improvement was achieved. We believe that our study would provide a key solution for achieving highly sensitive imaging sensor arrays based on sub-micron and low-dimensional photodetectors such as nanowires.

Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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