ACS Photonics

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Article

Strategy for Addressing the Low Quantum Efficiency of Nanowire Photodetectors

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Cite This: *ACS Photonics* 2022, 9, 2280−2286

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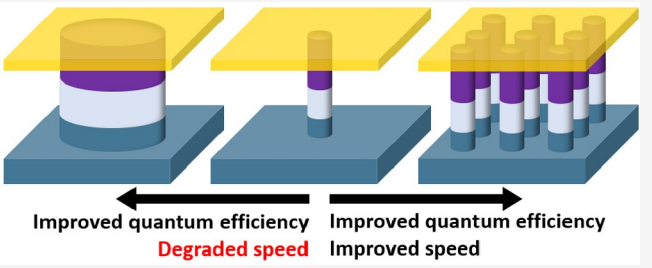
ABSTRACT: Nanowire photodetectors are attractive for their high speed and responsivity, enabled by small junction capacitance and high internal gain. However, their effectiveness is hampered by a low quantum efficiency due to poor light coupling to their intrinsically small size. The optically sensitive area can be increased by connecting arrays of standing nanowires (pillars) in parallel under a single readout, but the increase in dark current and total capacitance might reduce pixel sensitivity. The net effect has not yet been thoroughly investigated. In this work, we prove that such multipillar architecture indeed improves effective pixel sensitivity without reducing speed. Our theoretical analysis reveals that the pixel response time is dominated by the constituent nanowires rather than by the global capacitance, resulting in improved quantum efficiency for equivalent speed. We simultaneously characterize different pixel designs on a single focal plane array, demonstrating the viability of multipillar architectures for large-area detectors and imagers.



KEYWORDS: *low-dimensional, nanowires, photon detectors, quantum efficiency, infrared, collection efficiency*

INTRODUCTION

Semiconducting nanowire photodetectors have represented one of the most attractive technologies for light detection and imaging for the last few decades, thanks to their unique physical properties enabling large responsivity, low dark current, and low voltage operation near and at room temperature. Several nanowire photodetectors have been reported achieving exceptional performance across the visible, UV, and infrared.[1−3] Owing to their promising performance as individual photodetectors, considerable effort has been dedicated to the integration of nanowires into large sensors and arrays for applications in imaging, spectroscopy, and other multimode optical systems.[4−7]

However, the main challenge for the implementation of large-area detectors and imagers based on nanowire photodetectors is the poor coupling between the nanowire volume and the light incident across the detector area, resulting in extremely low quantum efficiency.[8−12] In imaging, as an example, the mismatch between the nanoscale size of the nanowire and the micron-scale pixel size of common CMOS readout circuitry leads to poor pixel collection efficiency and sensitivity.[13]

Viable strategies for enhancing light coupling to the nanowires include microlenses,[14] metalenses,[15] or waveguiding.[16] These approaches can only partially solve the problem, given the intrinsic losses related to the focusing of light beyond the diffraction limit. On the other hand, densely packed arrays of vertically standing nanowires (pillars) can provide a boost to quantum efficiency by increasing the optical collection area.[3,17−22] However, the increase in total junction area as well as surface-to-volume ratio of such arrays compared to individual nanowires may lead to a decrease in pixel sensitivity.[13] The net effect on pixel performance is thus not easily predicted and has not yet been investigated, leaving an open question on the viability of this design strategy for the implementation of large-area nanowire detectors with high quantum efficiency.

In this work, we investigate a pixel architecture consisting of arrays of standing nanowire phototransistors connected in parallel within the same pixel of the CMOS readout (multipillar pixel). Similar to most nanowire photodetectors, these phototransistors have internal gain that amplifies photoresponse to enable detection with high signal-to-noise ratio. We fabricated an infrared focal plane array of InGaAs/InP nanowire phototransistors, with 320 × 256 pixels each containing arrays of 1−49 nanowires. We show that this architecture enhances the quantum efficiency of the pixel

Received: January 5, 2022
Published: June 30, 2022

without compromising the unique detection properties of the nanowire phototransistors. In particular, our measurements show that the pixel response time is determined not by the number of nanowires in the array but by the capacitance of the individual nanowires. We present a simple analytical model to help explain this useful phenomenon.

Interestingly, a conceptually similar strategy has also been employed in some state-of-the-art large-area avalanche photodiodes (APD), where the pixel area is divided into a few smaller photodiode structures connected in parallel in order to reduce the noise and capacitance of the pixel.[23−25] These isolated APD structures (obtained by isolation etching of the conventional APD pixel mesa) measure several microns in size and retain the same properties of the bulk material. To the best of our knowledge, there is no reported experimental demonstration or theoretical evaluation of multipillar pixel architecture based on nanowire photodetectors, and this work is the first comprehensive investigation of this design strategy and its first implementation into a large-area imaging focal plane array. The strategy presented in this work can constitute a viable solution to improving the quantum efficiency and sensitivity of nanowire photodetectors, and lead the way toward large-area detectors and imagers that leverage the unique properties of nanowires.

FOCAL PLANE ARRAY BASED ON MULTIPILLAR PIXELS

In order to investigate the efficacy of the multipillar architecture, we fabricated a focal plane array (FPA) containing different types of single-pillar and multipillar nanowire phototransistor pixels, shown in Figure 1. The heterojunction phototransistor (HPT) epitaxial design consists of an NPN structure based on the InGaAs/InP material system, similar to those reported in our previous work.[26] For a detailed description of the epitaxial design as well as the device fabrication process, we refer the reader to the Supporting Information. Notably, a special fabrication technique was developed in order to be able to connect large numbers of nanowire phototransistors spanning the majority of the pixel area (30 × 30 μm in this case) while maintaining the ideal size of the indium bump to ensure high-yield flip-chip bonding (around 10 μm in diameter), which is also discussed in detail in the Supporting Information.

The FPA depicted in Figure 1 was specifically designed to investigate the effects of two different strategies for improving the pixel quantum efficiency. The first is increasing the diameter of the phototransistor pillars to cover a larger portion of the pixel area. For this, we included pixels consisting of single phototransistor structures of increasing diameter (1−8 μm). The second strategy is the multipillar pixel architecture presented above. For this, we included pixels consisting of an increasing number of phototransistor structures 1 μm in diameter (single-pillar to 7 × 7 multipillar) connected in parallel under a single indium bump. When the FPA is hybridized with the read-out circuitry (ROIC) via flip-chip bonding, these pillars form a single pixel, as shown in Figure 1b,c.

Crucially, the various pixel designs are intermixed across the same FPA, as shown in Figure 1a, and all pixel types undergo the same processing on the same sample. This rules out potential variations due to growth nonuniformity or different fabrication runs and enables investigations to be performed under identical conditions. Finally, we also fabricated additional FPAs to investigate multipillar pixel architecture with a range of individual pillar sizes, ranging from 200 nm to 2 μm. As presented in the Supporting Information, the fundamental findings presented in the following sections were also confirmed for these pixels with different pillar diameters.

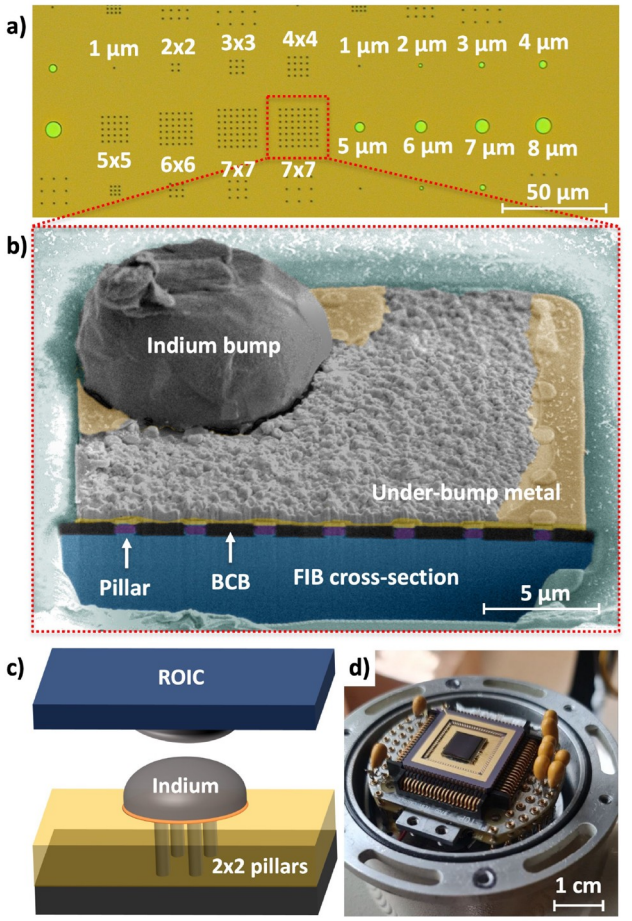


Figure 1. Focal plane array based on multipillar pixels. (a) Microscope image of several pixels on the fabricated FPA, where the area of a single pixel is exemplified by the square defined by the red dashed line. As shown in this image, this FPA includes both pixels with varying number of nanowires (1 × 1 to 7 × 7) as well as pixels with detector pillars of increasing diameters (1−8 μm). (b) False colored cross-sectional FIB-SEM image of a 7 × 7 multipillar pixel (such as the one in the red dashed square in (a), hybridized under a single indium bump. (c) Schematic of the flip-chip indium bump bonding process employed to hybridize a multipillar pixel sensor to the corresponding pixel on the ROIC. (d) Picture of the focal plane array mounted and wire-bonded to a chip carrier and installed in a dewar for characterization.

QUANTUM EFFICIENCY AND SPEED OF MULTIPILLAR PIXELS

The key performance parameters governing the sensitivity of a pixel photodetector are its quantum efficiency, noise level, and response time.[13,27] An example of the improvement in quantum efficiency enabled by the multipillar pixel architecture is offered by the measured photoresponse maps shown in the Supporting Information. The net effect of this design on the pixel sensitivity, however, is not obvious, since the increase in total junction area as well as surface-to-volume ratio of such arrays compared to individual nanowires can result in higher

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ACS Photonics 2022, 9, 2280−2286

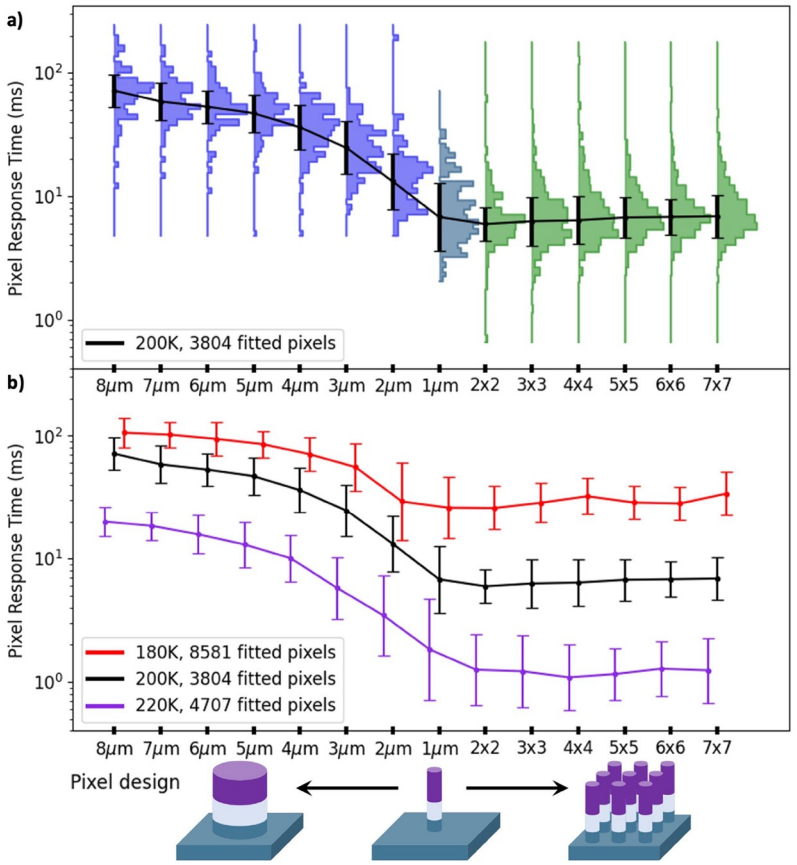

Figure 2. Exponential response time of different pixel designs on the same FPA. (a) Sideways histograms showing the distribution of individual pixel response times at 200 K, grouped by pixel design. The mid point on the horizontal axis corresponds to a single nanowire 1 μm in diameter; to the right are multipillar pixels consisting of 2 × 2 to 7 × 7 nanowires all 1 μm in diameter, while to the left are pixels consisting of single pillars from 2 to 8 μm in diameter. The speed of the single-pillar designs increases with pillar diameter, but the speed of the multipillar designs is independent of number of pillars. (b) The same trend in response time holds even as temperature is varied. In both plots, the solid line represents the mean of a Gaussian fitted to the performance distribution, with vertical bars representing one standard deviation.

dark current and device capacitance. Therefore, in order to investigate the viability of the multipillar design strategy for high-sensitivity large-area detection and imaging, we performed a comprehensive characterization of the pixel performance metrics of all different pixel types across the FPA.

Time-resolved photoresponse measurements were performed using a calibrated pulsed SLED source with a peak emission wavelength at 1550 nm to illuminate all FPA pixels simultaneously with uniform diffused light through the polished transparent InP substrate. An exponential rise and fall time was fitted to the measured time-resolved photoresponse of each pixel to obtain the response time of that pixel. Figure 2 shows the distribution of response time across different pixel types, showing the effect of different pixel designs on the speed of the devices. In pixels consisting of a single phototransistor structure, increasing the pillar diameter from 1 to 8 μm results in slower device photoresponse (center-to-left in Figure 2a). As expected, the measured response time increases proportionally to the cross-sectional area of the pillar, confirming that the speed of the devices is dominated by the junction capacitance.[13,28] The other side of Figure 2a (center-to-right) shows the effect of increasing the number of nanowire phototransistors in the multipillar architecture, while keeping the diameter of each pillar constant at around 1 μm. Interestingly, increasing the number of nanowire phototransistors showed no significant effect on the device speed, which is independent of the number of pillars within a pixel (ranging from 1 to 49). Figure 2b shows that these effects are replicated at all three temperatures we investigated.

This phenomenon is somewhat surprising, given that the overall cross-sectional area of these multipillar pixels is equivalent to that of larger single-pillar pixels. The effect can nonetheless be explained with a simple analytical model considering each individual nanowire phototransistor as an independent current amplification source. Like many photodetectors, two-terminal phototransistors such as the ones employed in this work operate with a floating base layer, whose potential is modulated by the photogenerated minority carriers to produce an internal amplification gain,[26,29] as depicted in Figure 3a. Here, the signal amplification and response time are governed by the capacitance of the base-emitter junction C_{BE}.[30]

In a multipillar pixel, despite all phototransistors being connected in parallel at the two terminals, the base potential governing the current amplification is floating, as depicted in Figure 3b. As a result, the amplification in each individual nanowire phototransistor is carried out independently and thereby only governed by its own base capacitance. All the amplified photocurrents then add in parallel at the pixel terminals, so the total photoresponse current output of a pixel with N pillars to a step-like pulse of light with N_{ph} photons per response time is expressed by

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ACS Photonics 2022, 9, 2280−2286

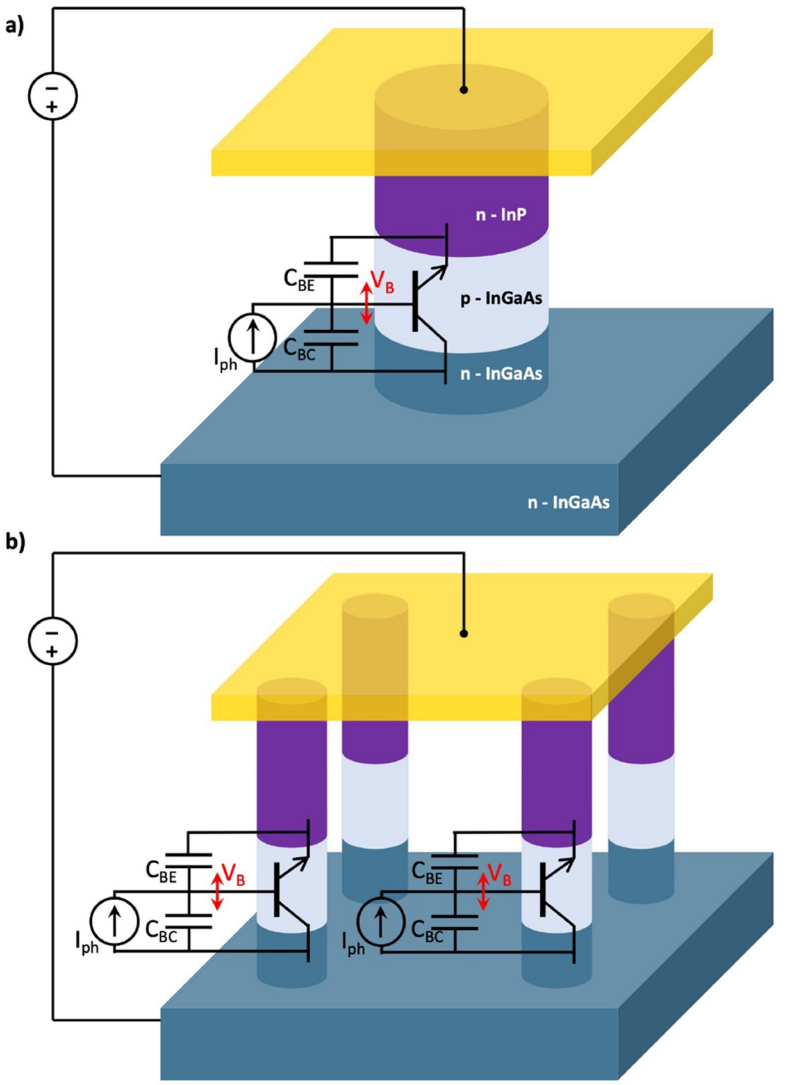

Figure 3. Schematic depiction of the detection and amplification mechanisms in pixels consisting of single pillar (a) and multipillar (b) nanowire phototransistors. The amplification gain of the photogenerated current (I_{ph}) is achieved via modulation of the base layer potential (V_B), which is floating, and is governed by the capacitance of the base junctions (C_{BE} and C_{BC}). In a multipillar pixel (b) the amplification in each individual nanowire is carried out independently and the amplified photocurrents are added in parallel.

$$I_{ph}(t) = \left(1 - \exp\left(\frac{-t}{r_d C_{BE}}\right)\right)\sum_{i=0}^{N} I_S\left(\exp\left(\frac{q^2 \eta_i N_{ph}}{C_{BE_i}\eta_F kT}\right) - 1\right) \quad (1)$$

Here, r_d is the dynamic resistance, I_S is the saturation current as defined in ref 30. q is the fundamental charge, η_i is the quantum efficiency of the ith nanowire, η_F is the ideality factor, k is Boltzmann's constant, and T is the temperature. A detailed derivation of eq 1, together with definitions of the above-mentioned quantities, can be found in the Supporting Information.

Importantly, the capacitance term C_{BE_i} in eq 1, governing the photoresponse of multipillar pixels, refers to the capacitance of each individual pillar and not to the overall capacitance between the pixel terminals. Since all individually amplified photocurrents add in parallel at the pixel terminals, the global pixel response time will be the average of the response times of the individual nanowire phototransistors, illustrating why the response time shown in Figure 2 is not affected by the number of pillars but only by their size (i.e., individual capacitance). By using the nanowires diameter to estimate C_{BE}, this model yields estimated values for the amplitude and speed of the photoresponse of different pixels types that are in good agreement with those measured across the FPA, as shown in the Supporting Information. For a more accurate modeling of the pixel photoresponse, the parasitic effects of surface leakage and fringing capacitance can be included in the model: their effect is related to the ratio of the respective shunt resistance and fringing capacitance to the internal resistance and capacitance of the nanowire detectors, as discussed in the Supporting Information.

It is important to note that this model and its main findings are also valid for nonuniform size distributions of the pillars within a multipillar pixel. Due to the physics involved, the individual sizes of each of the pillars in a multipillar pixel contribute to governing the photoresponse speed and amplitude of the pixel. As a result, the model can be used for estimating the performance of multipillar pixels based on any given nonuniform pillar distribution. This is especially

https://doi.org/10.1021/acsphotonics.2c00029
ACS Photonics 2022, 9, 2280−2286

relevant for nanowire detectors fabricated from bottom-up techniques, which typically exhibit broader size distribution compared to those fabricated from top-down fabrication methods.[18,31]

Finally, this model is not restricted to this particular class of floating-base phototransistors, but extends to a large number of two-terminal nanowire photodetectors that employ similar mechanisms to produce internal gain, such as by the modulation of Schottky barrier or surface depletion.[2,32−35]

EFFECTIVE PIXEL SENSITIVITY

It is rather customary in the low-dimensional photodetector community to report the sensitivity of novel detectors by normalizing to the size of the detector structure. In thin film photodetectors, for example, this is sometimes done by estimating the absorption across the thickness of the absorbing material and computing the fraction of incident light available to cause a photoresponse.[36] In nanowires photodetectors, the sensitivity is typically normalized to the ratio of cross-sectional area of the nanowire to the total illuminated area.[8−12] Aside from leading to sensitivity mischaracterization in situations where the absorption of nanowires extends beyond the nanowire diameter (due for instance to effects like wave-guiding[16] or diffusion length), this approach is certainly misleading for imaging applications. The size of the pixel is often constrained by the ROIC to a few microns or larger[27] and the uniform incident light cannot be effectively coupled to a nanoscale photodetector without considerable losses. Even when microlens or metalens arrays are employed, they do not ensure a perfect coupling of flat-field incident light to a nanoscale volume, and the lens efficiency and fill factor should be taken into account.[14,15] As such, we strongly advocate for all photodetector work, especially when related to imaging, to report sensitivity metrics as measured across the full area of the pixels.

When considering the effective sensitivity of a pixel, multipillar pixels are designed to out-perform single-pillar pixels having equal total cross-sectional area. Specifically, the trade-off between speed and quantum efficiency dictated by the phototransistor junction capacitance limits the sensitivity of pixels based on a single-pillar architecture. In contrast, the multipillar pixel architecture preserves the speed of small nanowire phototransistors while the increased number of pillars enables an improvement in pixel quantum efficiency, resulting in an overall improvement in effective pixel sensitivity. In addition, multipillar pixels can be used at higher frame rates without sacrificing effective responsivity thanks to their faster response times.[37] Finally, multipillar geometries will benefit more than single pillars from situations where the absorption extends beyond the pillar diameter.[16]

To evaluate the pixel performance in a realistic situation, the FPA was uniformly illuminated across all pixels by a 143 Hz square wave, with each pixel receiving 1.4 pW across its 30 μm × 30 μm surface. The signal-to-noise ratio (SNR) of each pixel was calculated by finding the peak-to-peak response between the light and dark frames and dividing by the standard deviation among the light frames: the results for approximately 4050 responsive pixels are shown in Figure 4. At 220 K, the larger diameter phototransistor pillars (≥4 μm) cannot fully respond to signals faster than ∼50 Hz (see Figure 2b). This translates to decreased response to the 143 Hz square wave as compared to a single 1 μm pillar, as seen on the left half of Figure 4. In contrast, the multipillar pixels remain functional up

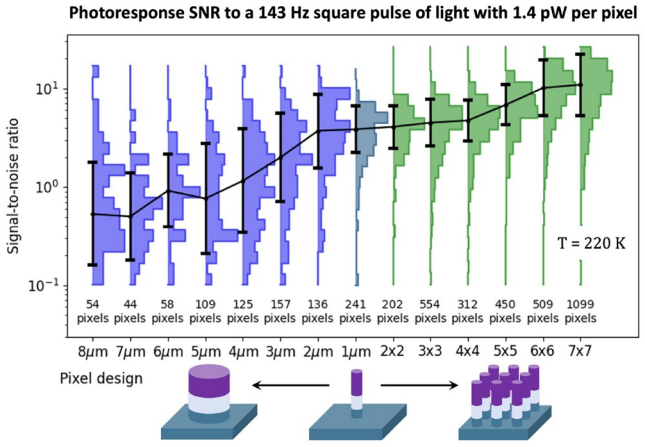

Figure 4. Comparison of signal-to-noise ratio of the photoresponses of different pixel types on the same FPA at 220 K, illuminated by a 1.4 pW square wave pulsed at 143 Hz. Pixel types are labeled as in Figure 2, with the total number of pixels characterized for each pixel type reported near the bottom of the figure. The solid line represents the mean of a Gaussian fitted to each sideways histogram of pixel performances, with vertical bars representing one standard deviation.

to ∼400 Hz. In parallel, the coverage from additional pillars increases absorption for larger arrays of nanowires, leading to increased SNR for larger arrays on the right half of Figure 4. In this realistic metric of attempting to detect a time-varying signal at a given frequency and power, this result demonstrates the viability of the multipillar pixel design in imaging contexts.

CONCLUSION

In this work, we demonstrated a viable strategy for the application of nanowire photodetectors in large imaging sensors, consisting of arrays of nanowires spanning the entire area of the pixel and connected in parallel to the same readout pixel. We confirmed the effectiveness of this architecture by fabricating a focal plane array consisting of different pixel architectures. Most notably, the pixels consisting of arrays of nanowires connected in parallel enable an enhancement in quantum efficiency compared to pixels consisting of a single nanowire, while preserving a fast photoresponse compared to nanowires of larger diameter. As a result, these pixels exhibit an overall improvement in sensitivity to the light incident across the entire pixel area. The proposed strategy can open new avenues for the implementation of large-area detectors and imagers based on nanowire photodetectors, potentially revolutionizing a vast number of applications by leveraging the extraordinary detection capabilities of nanowires.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsphotonics.2c00029.

Details of the epitaxial design and fabrication process of the focal plane array. Photoresponse map of the quantum efficiency enhancement of multipillar pixels. Full derivation of the device model and corresponding model fit to measured data. Modeling parasitic resistance and capacitance. Dark current distribution measured across different pixel types. Experimental details of the characterization of the pixels effective sensitivity and

https://doi.org/10.1021/acsphotonics.2c00029
ACS Photonics 2022, 9, 2280−2286

SNR. Investigation of multipillar pixel architecture based on different pillar diameters (PDF)

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Author Contributions

‡S.B. and J.R. contributed equally to this work.

Funding

This work was supported by W. M. Keck Foundation under a Research Grant in Science and Engineering. This work was performed, in part, at the Center for Nanoscale Materials of Argonne National Laboratory. The use of the Center for Nanoscale Materials, an Office of Science user facility, was supported by the U.S. Department of Energy, Office of Science, Office of Basic Energy Sciences, under Contract No. DE-AC02−06CH11357. S.B. gratefully acknowledges support from the Ryan Fellowship and the International Institute for Nanotechnology at Northwestern University.

Notes

The authors declare no competing financial interest.

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https://doi.org/10.1021/acsphotonics.2c00029
ACS Photonics 2022, 9, 2280−2286